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Switchable, Auto Gain Amplifier

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Switchable, Auto Gain Amplifier

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ABSTRACT

An electronic amplifier capable of automatically reducing its gain to avoid output saturation is described. Design goals, electrical schematic, and samples of output waveforms are included.

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Switchable, Auto Gain Amplifier

INTRODUCTION

When recording data from single-event field experiments it is often difficult to estimate the signal levels that may be generated by various sensors. A desirable recorded signal would be one whose amplitude is not saturated but nearly full scale. This gives the optimum signal-to-noise ratio for data analysis purposes. An amplifier gain that is too low will result in only noise being recorded, whereas too much amplifier gain will produce saturated signals whose pulse shape and amplitude are lost. To overcome the uncertainties of predicting proper gain settings, an amplifier that selects its own gain setting was designed and built. That Switchable, Auto Gain Amplifier (SAGA) is the subject of this report.

AMPLIFIER REQUIREMENTS

Data for a recent field test series were to be recorded using digitizing oscilloscopes capable of storing the recorded waveforms on removable bubble memory cartridges. Each oscilloscope channel was to be digitized with eight-bit resolution and could be sampled at rates as high as 10 megasamples/s. The data to be recorded were pulses requiring a preamplifier electrical bandwidth of 1 MHz. The goal for SAGA was to switch to lower output gains in a time comparable to the minimum data-sampling time interval of 100 ns. Since data sampling was to be asynchronous with gain switching, it was realized that one or more sampled data points might be invalid each time a gain switch occurred.

Previous similar experiments were conducted using a preamplifier with manually selectable voltage gains of 1, 10, and 100. Field use of this preamplifier indicated a need for more closely spaced gain settings as well as a wider range of possible gains. To make the amplifier useful for a variety of applications, provisions were made for inputs from either a 0.5-mA current source or a voltage source of up to 10 V. Both positive and negative input polarities were to be accommodated. The output was to drive a coaxial cable terminated in 50 Ω. The resulting amplifier card was to be no larger than 5 inches square.

AMPLIFIER DESIGN

The electrical schematic of SAGA, as built, is shown in Figure 1. Integrated circuit AD509 operational amplifier chips had been used successfully in previous applications. Electrical

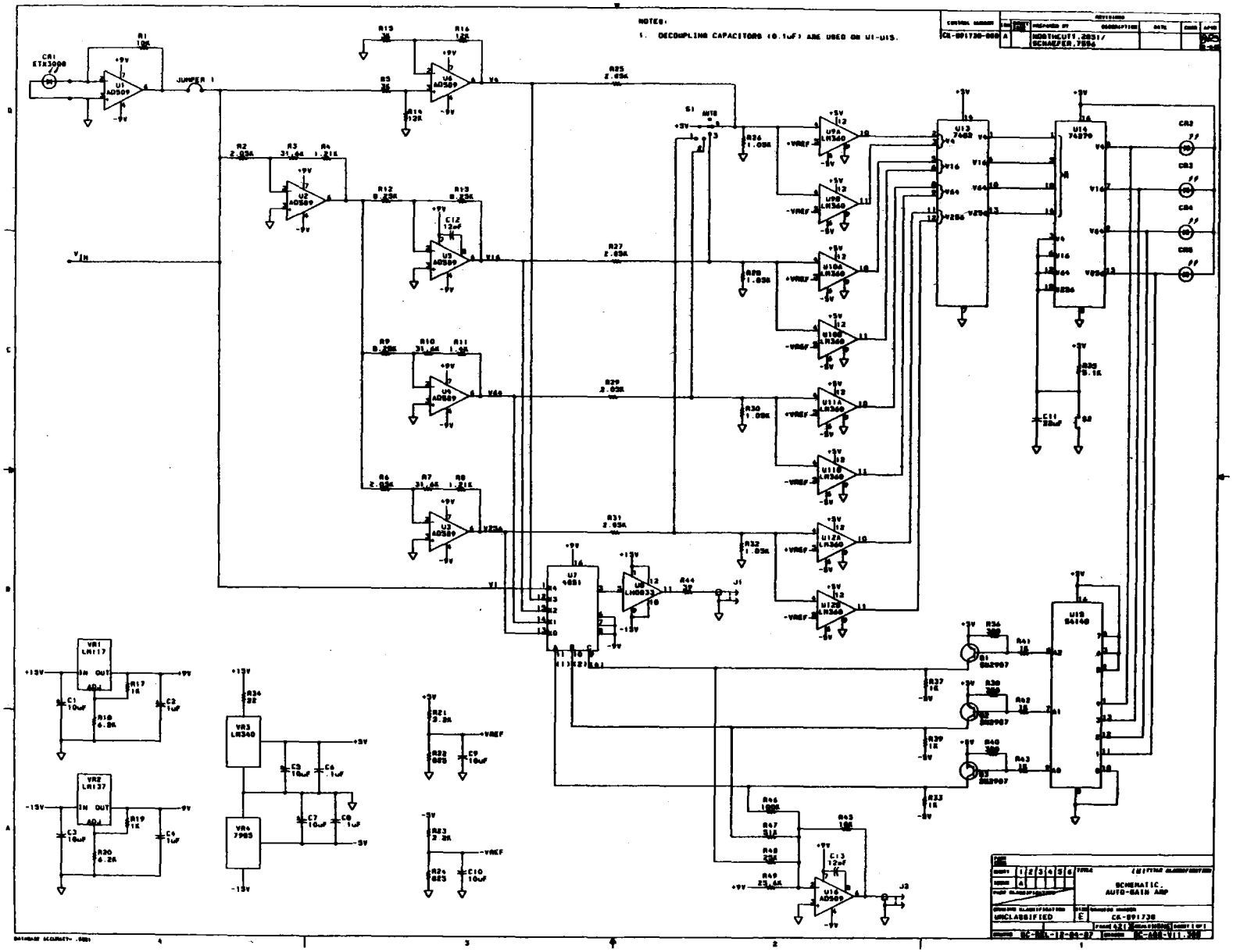

Figure 1. Electrical Schematic Diagram of SAGA

bandwidth of the AD509 was adequate for this application at a reasonable noise level. Faster circuits are, in general, more noisy, whereas the quieter circuits do not have the desired bandwidth. A certain level of noise could be tolerated since, by switching its gain, the amplifier would maintain a larger output signal than otherwise. Also, the resolvable output voltage levels were limited by an eight-bit digitizer. The circuit descriptions that follow refer to components by the designations found in Figure 1.

U1 is a single-stage transimpedance preamplifier for direct input of currents with a gain of 10 V/mA. The output of U8 is limited to a linear region of ±5 V. With unity voltage gain in the following amplifier stages, this results in a maximum useful input current range of ±0.5 mA. The gain of the transimpedance amplifier is directly controlled by resistor R1. Other current-to-voltage gains, within reason, can be achieved by choosing the appropriate R1 value.

By removing jumper J1, a voltage signal can be input directly at V_{in}. The analog multiplexer, U7, has five inputs, each a different amplified version of V_{in}. V1 is identically V_{in}, the 1 indicating V_{in} X 1. The additional four signals, V4 through V256, are produced by four parallel amplifier chains. The signal selected for the output buffer, U8, will be 1, 4, 16, 64, or 256 times V_{in}. Voltage limitations of the analog multiplexer, U7, restrict the usable input to the unity gain buffer to ±5 V, although U8 itself is capable of ±10 V. In order to maintain electrical bandwidth, each individual amplifier chip has a maximum gain of 16. Similarly, to avoid large phase delays and distortion of the output signals, there are no more than two amplifier chips in any of the amplifier chains.

With a gain-switching amplifier a high gain can initially be selected to better record small signals. If the signal exceeds a threshold such that saturation is possible, the gain can be reduced automatically, allowing more dynamic range. Such a system could be arranged to decrease gains as the signal levels fall below a lower voltage threshold. SAGA is intended to be used with pulses of a few microseconds duration. The gain for a fast-rising pulse can be quickly lowered by selecting an amplifier chain of lower gain. Without circuit modifications the higher-gain amplifier chains will go into saturation. Switching rapidly to a higher-gain, saturated amplifier as a fast pulse falls will be futile. The resulting output will represent only the saturation recovery of the higher-gain amplifier. The complications of preventing saturation, or of determining when the higher-gain amplifiers come out of saturation, determined that SAGA can only decrease gains automatically. Any gain increases must be by manual means.

Each of the voltage signals V4, V16, V64, V256 are input to two of the eight voltage comparators, U9A-U12B. Four of the comparator outputs switch at +4 V; the other four switch at -4 V. The NOR gates of U13 combine the signals from the + and - comparators to indicate when the voltage for a particular gain goes out of the permissible +4 to -4 V window. In this way pulses of either polarity can produce the proper gain reductions. The combined comparator outputs from U13 are used by U14 and U15 to determine which multiplexer input signal to select as the output signal. Any pulses from U13 indicating voltage levels above threshold are latched in U14. This latching does the function of allowing gains to decrease but not increase. Threshold levels are set at 4 V to allow gain switching to occur on fast-rising signals before output saturation at 5.5 V.

U14 also drives four LED indicators that give a visual indication of gain. The highest gain used with the lowest signal levels has no LEDs on, whereas the lowest gain, corresponding to the largest signal, has all four LEDs illuminated. The Reset switch, S2, resets the four latches of U14, extinguishing all LEDs and selecting the highest gain. If the input signal is of sufficient magnitude because of background signals, input offsets, etc., the gain may switch to a lower level immediately upon releasing S2. Instead of referring to the actual voltage gain of the SAGA, which may be nebulous for current inputs, gains are referred to by the number of illuminated LEDs. The highest gain is referred to as Gain 0, because 0 LEDs are lit, instead of by the internal voltage gain of 256. By this convention, a small signal input could use a Gain 0 whereas a large signal would require a Gain 4.

The priority encoder chip, U15, converts the gain LED signals into a binary code that selects the proper analog multiplexer signal. The U15 outputs are standard TTL levels. The multiplexer is wired with ±9-V supply voltages to make the inputs and output usable over a ±5-V range. With these supply voltages, the logic input signal must also be bipolar. Q1, Q2, and Q3 are transistor switches that convert the TTL logic levels of U15 to ±5 V logic levels for use by U7.

If the amplitude of a signal is known to be sufficiently large that maximum gain is not required, the Gain Select switch, S1, can be used to prevent the higher gains from being used. This might be desirable to avoid the higher noise levels inherent with higher amplifier gains. S1 is a multiposition switch with five usable positions: Auto, 1, 2, 3, and 4. In the Auto position, SAGA is fully automatic. After a Reset, the gain will be at the highest level possible with the input offset voltages. As the input signal rises, all gain levels are used as the gain is switched lower. In the other S1 positions, the initial gain is reduced. The initial gain is forced to be at least a gain

equal to the number of the setting. A Gain Select of 1 will force the highest gain to be no higher than Gain 1; Gain 0 cannot be used. A Gain Select of 3 will prevent use of Gains 0, 1, and 2. A Gain Select of 4 will force SAGA to remain in its lowest gain setting, Gain 4, no matter what the input signal amplitude. All settings except Gain Select 4 allow switching to lower gain levels should the input signal become large. (No matter what Gain Select switch setting or input signal is present, as long as the Reset button is depressed, the output will be at the the highest possible gain, Gain 0.)

The Gain Select switch functions by applying +5 V directly to the input of the appropriate + comparator forcing the comparator to signal a threshold condition. The comparator signal not only lights its corresponding LED, but also reduces the selected gain. Normally, the gain LEDs will come on in the order 1, 2, 3, and finally 4 as the input signal increases. The fourth gain LED will normally be on only if the three other LEDs are also on. A numerically high Gain Select switch setting, combined with a low input signal, can cause a high numbered LED to be on without any of the lower numbered ones. This is because the forced condition on the comparator was not produced by a normal comparator switching sequence. The priority encoder operates in a manner such that the output gain corresponds to the highest numbered LED illuminated, even if lower numbered LEDs are not on.

Initial difficulty in reconstructing analog signals from the digitized outputs from U8 indicated the need to provide an output indicating the gain selected. In addition to the normal voltage output from U8 (J1), SAGA also has a gain output from U16 (J2). The U16 gain output amplifier produces an analog voltage proportional to the number of LEDs illuminated: Gain 0 = 0 V, Gain 1 = -1 V, etc. Switching time of the U16 signal is comparable to the switching time of the multiplexed signal itself, i.e., 100 to 200 ns.

The U8 unity gain buffer is used to isolate the analog multiplexer from the output and to allow the capability of driving a 50-Ω scope load. The U16 Gain output, having only five allowed levels, does not need to be as faithfully reproduced and does not have such a buffer. Its output can only drive loads of 500 Ω or larger.

SAMPLE OUTPUT WAVEFORMS

The built-in versatility of the SAGA allows its use in a variety of applications with either voltage or current sources of positive or negative polarity. Its first application was as an amplifier of negative amplitude photodiode current pulses. The circuit card installed in that radiometer system is shown in Figure 2. The Gain Select and Reset switches as well as the two

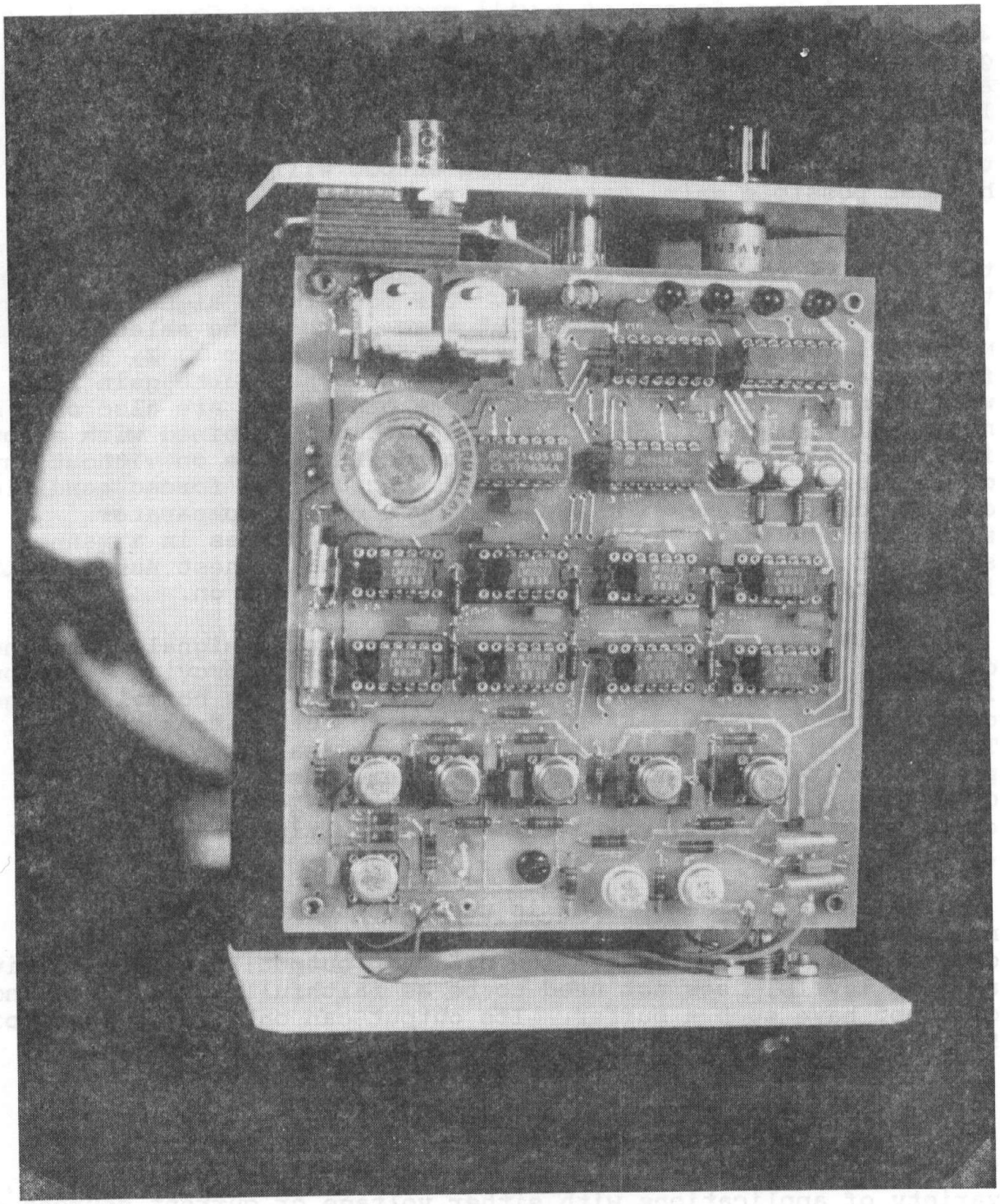

Figure 2. SAGA Circuitry Installed as Radiometer Amplifier

output BNCs are located at the top. Just below the Gain Select switch are the four gain-indicating LEDs. The connector in the lower right supplies ±15-V input power. Figure 3 is an exterior view of the package showing the external components except the power connector, which is hidden under the bottom right corner.

Sample outputs from SAGA recorded by an eight-bit digitizing oscilloscope are illustrated in Figure 4. With the gain initially at its highest value (Gain 0), a 0-to-5 V trapezoidal voltage pulse input was applied at V_{in}. The center trace represents the input waveform, the upper trace the auto gain voltage output, and the lower trace is the gain output. The signal generator used for this test was not particularly noisy; the noise levels at all gains were similar. Real detectors often add more noise to the signal. The noise levels at the higher gains are generally more noticeable than the noise levels at lower gains after switching.

Without the additional 256x initial gain it would have been difficult to detect the small negative offset preceding the pulse. As the voltage output rises above 4 V, the gain is reduced by a factor of 4. In this example the gain reduction was evident in the voltage output waveform. (Were the gain reduction not so evident, as would be the case for a square pulse, there would be more need for the stepped-gain output displayed as the bottom trace.) Three additional gain reductions were performed until unity gain (Gain 4) was reached. Once at Gain 4, signals that exceeded the linear output voltage limit of 5.5 V would have been clipped by the U7 multiplexer. The falling edge of the voltage output looks identical to the input since the circuitry allowed no automatic gain increases.

Figure 5 is an expansion of the rising edge of the Figure 4 signals. Gain changes of the analog multiplexer corresponding to a single binary LSB change, such as 0-1 and 2-3, are accomplished in approximately 100 ns. Those corresponding to changes in the higher bits, such as 1-2 and 3-4, require on the order of 200 ns. This difference in switching times may be attributable not only to the multiplexer but to the priority encoder as well. Specification sheets indicate that a CD4529 multiplexer chip should switch more quickly than the CD4051. Experiments with both chips revealed the CD4051 to be faster and better suited to use for SAGA. The measured switching times for the CD4051 of 100 to 200 ns were comparable to the specified 120 ns typical, 240 ns maximum. A faster switching multiplexer would be a necessary improvement to SAGA if sub-microsecond input pulses were desired.

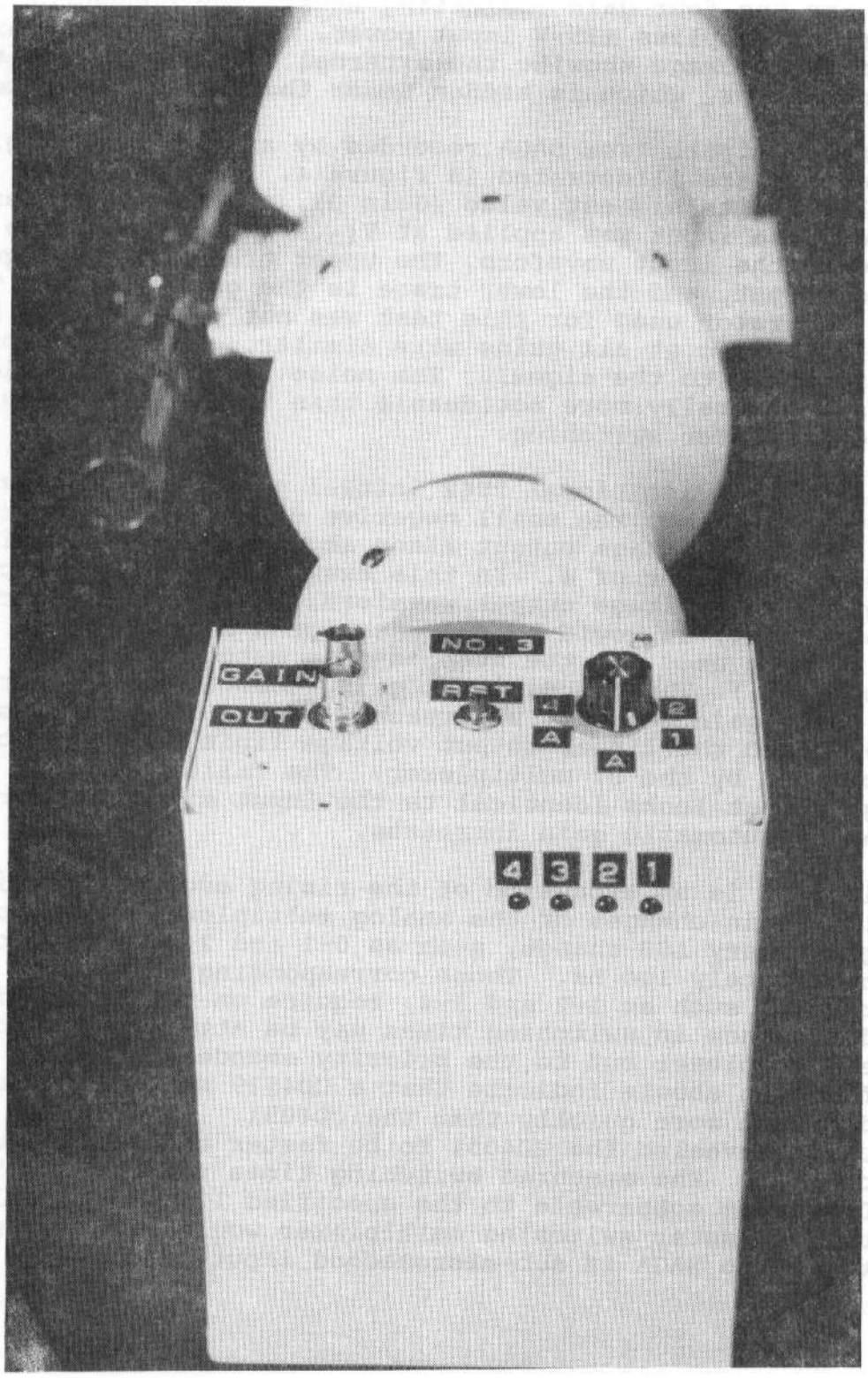

Figure 3. Exterior of SAGA Package

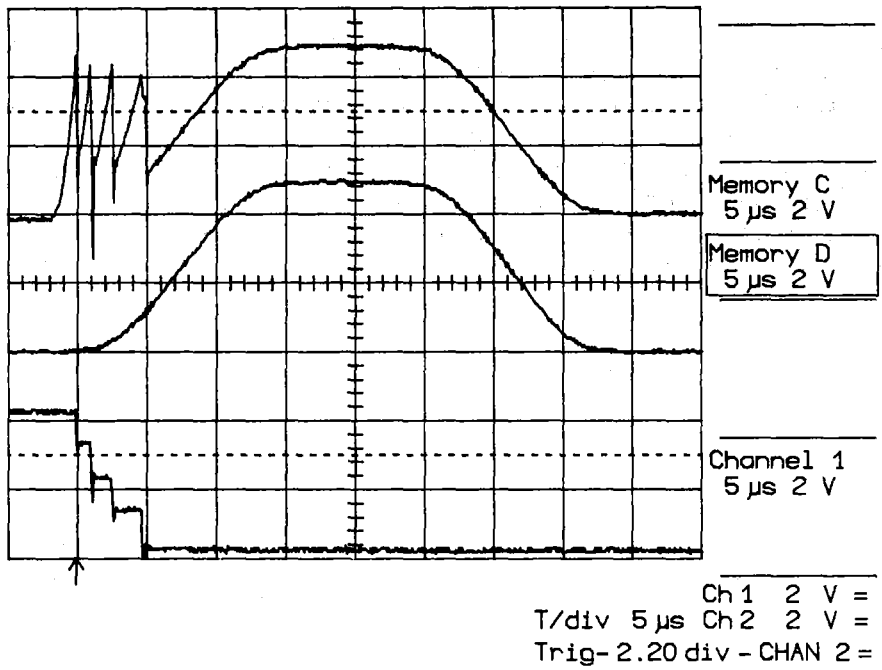

Figure 4. Sample of Input and Output Waveforms From SAGA

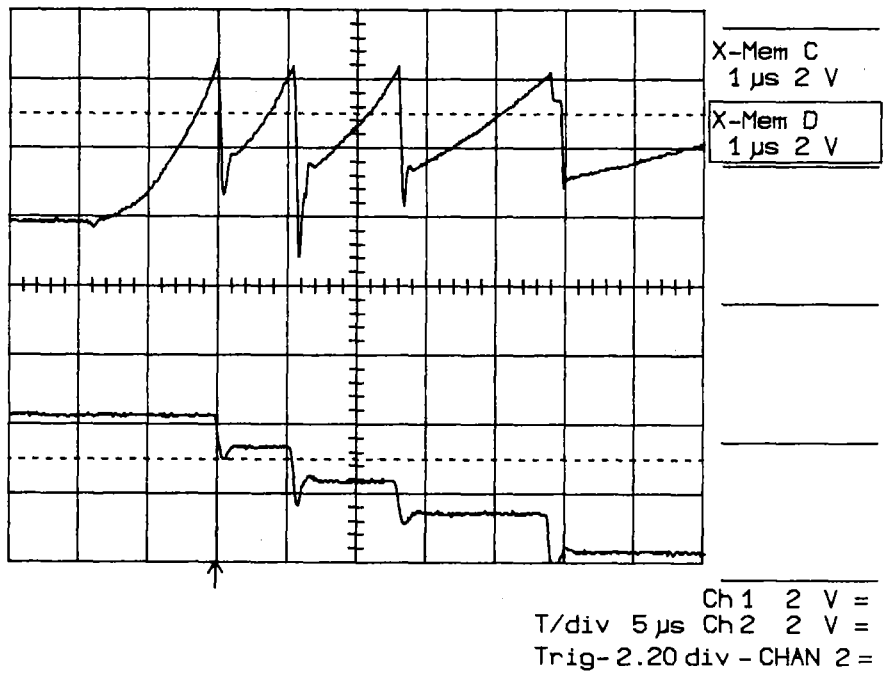

Figure 5. Expansion of Rising Edge of Figure 4 Pulse

CONCLUSIONS

An automatically switchable, gain-reducing amplifier for use with multi-microsecond pulses has been designed and built. Positive or negative inputs of current or voltage can be accommodated. As many as four gain reductions in steps of 1/4x are achieved each time the output voltage signal exceeds 4 V. Switching times between gains in the range of 100 to 200 ns are achievable with the current hardware. This amplifier has been successfully used to record field data on pulses several microseconds long.

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